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A New Configurable Full Adder For Low Power Applications

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ABSTRACT: Power consumption is a major issue for integrated circuit design. Adders are basic building blocks for any arithmetic logic design and are majorly used in DSP processor, where computations are done with adders. In this paper, we try to reduce the power consumption and area of the adder. In order to improve the performance of the digital computer system one must improve the basic 1-bit full adder cell. In this paper we analysis the 1-bit full adder using 9T full adder design. We proposed the design of exact adder with reduced area and reduced complexity at the transistor level.

KEYWORDS: Power dissipation, CMOS, Approximate full adder, Mirror adder, Body Bias logic.

I INTRODUCTION

Digital signal processing (DSP) is the backbone of various multimedia applications. Most of the DSP systems implement and give output in the form of either image or video for human consumption. Human beings having limited perceptual ability allows the algorithmic output to be numerically approximate rather than accurate. Conventional adder is one in all crucial elements of a processor that determines the output. In all electronics applications, 1-bit full adder is the basic gate utilized in arithmetic circuits like adders and multipliers. Thus, performance improvement of a complete adder block results in accurate general system performance. A full adder has three input and two output block within which the output square measure the addition of three input basic unit utilized in various circuits like parity checker, compressor and comparators. This uses high threshold voltage sleep junction transistors that cut-off circuit block once the block isn't change. The development of imprecise arithmetic circuit provide a layer of power reduction over conventional low power design. Previous work on logic complexity reduction have focused on algorithm, logic and gate level.

We propose logic complexity reduction at transistor level. The modification are applied at the bit level by simplifying mirror adder circuits. The approximate units not only have a reduced number of transistors, but it is also ensured that the internal node capacitances are reduced. Complexity reduction leads to power optimization in two ways. First, reduction in switched capacitance and leakage inherently. Second, it leads to shorter critical paths. Few works which focus on low power implementation with approximate computing at the algorithmic level include algorithmic noise tolerance (ANT) [3] and [6]. An error-tolerant adder operates by splitting the operand into accurate and inaccurate units is proposed in [11]. However, this technique does not leads to logic complexity reduction. A multiplier architecture uses a 2×2 inaccurate multiplier block results from simplified karnaugh map is given in [5]. Shin and Gupta [10] and Phillips et al. [8] also proposed logic complexity reduction by karnaugh map simplification.

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II RELATED WORK

A one bit full adder is having three single bit binary input (A, B, Ci) and two single bit binary output (SUM, Co). this full adder is highly scalable and found in many processing unit implementation. Other works focused on logic complexity reduction at the gate level are [12].

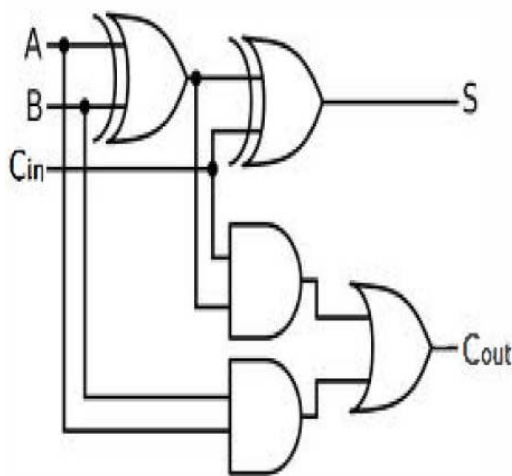


Fig.1: Logic Diagram of 1-bit Full Adder

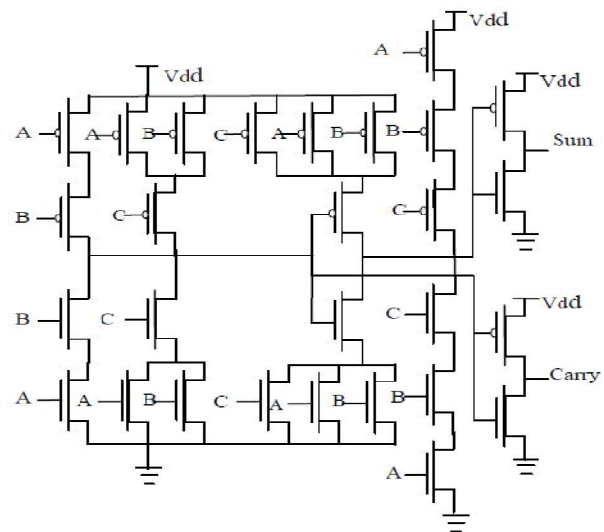


Fig.2: 28-T conventional Full Adder

$$\text{SUM} = \overline{A} B C_{\text{IN}} + \overline{A} B \overline{C}_{\text{IN}} + A B C_{\text{IN}} + A B \overline{C}_{\text{IN}}$$

$$\text{SUM} = A \text{ XOR } B \text{ XOR } C_{\text{IN}}$$

Fig. (1) and (2) shows the logic diagram and transistor schematic of the full adder. The circuit for given logic consists of 28 transistors (4 transistors used for the two inverters). Full adders acts as a fundamental building block component to larger units. So. Timing and power optimization at adder level can improve the circuit throughput ratings, speed enhancement and lowered power consumption.

A. Approximate Full Adder

In this section, we discuss several methodologies for designing approximate adders. In several approximations, multibit adders are splitted into two modules: one is upper part of more significant bits and the lower part of less significant bits. Since, mirror adder is one of the widely used economical implementations of full adder. A mirror adder is common as well as efficient adder. There are five different approximate mirror adder have been obtained from logic reduction at the transistor level. This reduction is done by removing some transistors.

B. Mirror Adder Strategies

The work that has been done prviously is based on the mirror adder strategy which gives procedures for various approximate mirror adder cell with less number of transistor. Faster charging/discharging of node capacitances can be obtained by removing some series transistor. This also leads to complexity reduction by reducing the αC term i.e. switched capacitance in $P_{\text{dynamic}} = \alpha C V_{\text{DD}}^2$ where α is the switching activity and C is the load capacitance being charged/discharged. Now, we discuss about the conventional mirror adder and its approximations.

C. Conventional Mirror Adder

Figure shows the transistor level which contains total of 24 transistors. It is based on complementary MOS logic. So, it is easy and advantageous to design approximations with this technique. When laying out the cell, the most critical issue is the minimization of the capacitance at node Co. The reduction of the diffusion capacitances is particularly important.

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The capacitance at node C_o is composed of four diffusion capacitances, two internal gate capacitances, and six gate capacitances in the connecting adder cell.

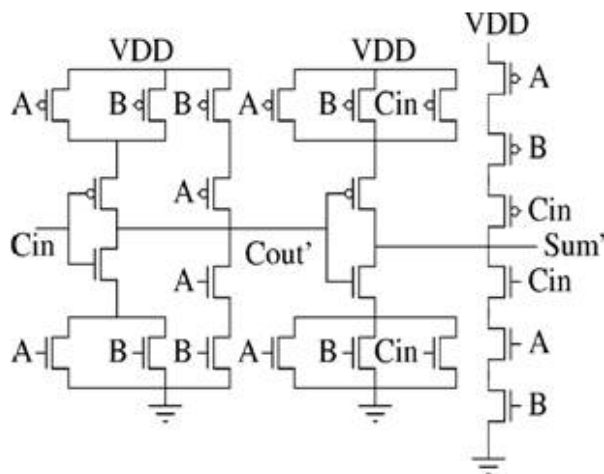


Fig.3: Conventional Mirror Adder

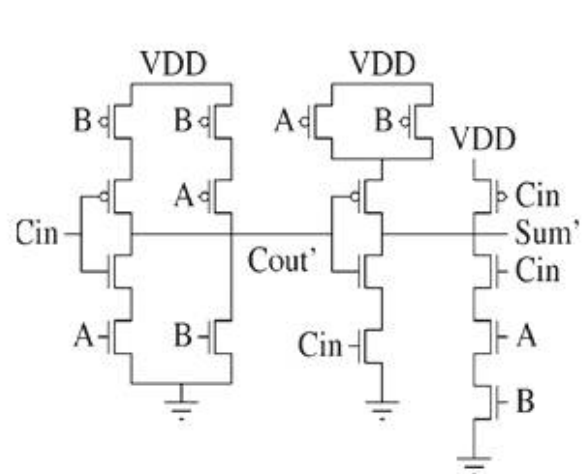


Fig.4 : Approximation Mirror Adder 1

D. Approximate Mirror Adders

We remove transistors from the conventional circuit one by one but not in arbitrary fashion. We get first approximation mirror adder by this method. We ensure that it does not result in any kind of short or open circuits in the modified schematic. This resulting simplification introduces less errors in the truth table. Fig.4 shows the CMOS circuit of approximate mirror adder 1.

The truth table of FA shows that $Sum = C_{out}'$ for six out of eight cases, except for the input combinations $A = 0, B = 0, C_{in} = 0$ and $A = 1, B = 1, C_{in} = 1$. In the conventional mirror adder C_{out} is computed in first stage. So, as given in fig.5 to get next approximate schematic we set $Sum = C_{out}$. However, a buffer stage is introduced to produce same function after C_{out} .

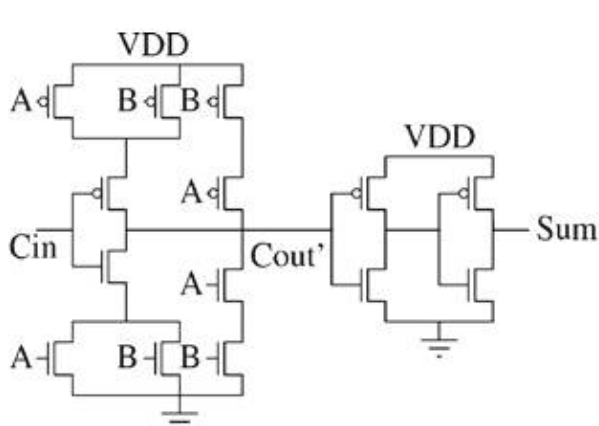


Fig.5 : Approximation Mirror adder 2

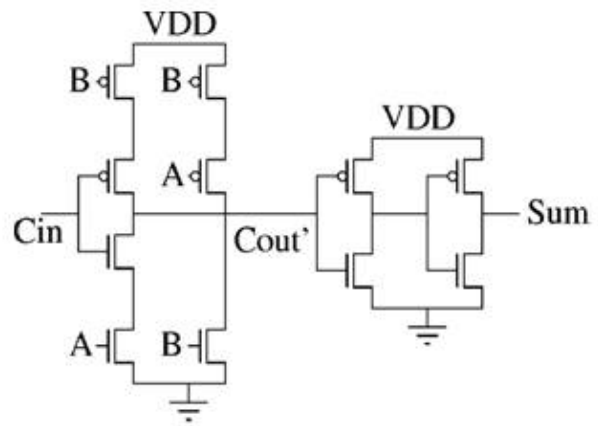


Fig.6 : Approximation Mirror Adder 3

International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 5, Issue 2, February 2016

The third approximation is combination of approximate mirror adder 1 and 2 shown in fig.6. This simplified schematic introduces three and one errors in Sum and C_{out} respectively. As the fig.7 shows, in the fourth approximation mirror adder $C_{out}=A$ for six out of eight cases given in the truth table. The Sum is calculated same as in the first approximation and for C_{out} an inverter is used. This simplification introduces two errors in C_{out} and three errors in Sum.

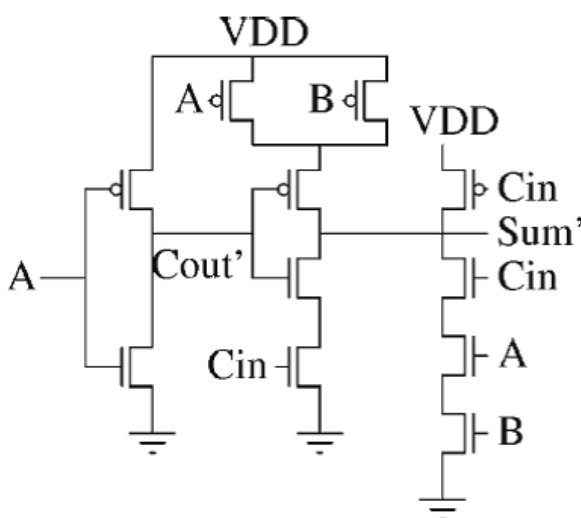


Fig.7 : Approximation Mirror adder 4

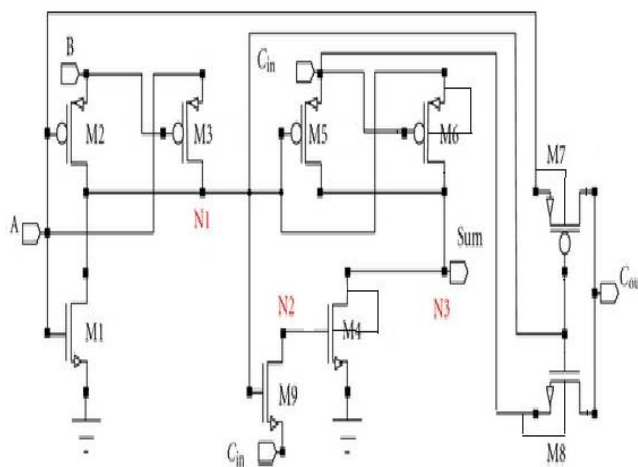


Fig.8: 9 Transistor Full Adder with Self Biasing

III. PROPOSED FULL ADDER

The 9 transistor full adder given in figure 8 is different from the conventional circuit. In this full adder the three input bits A, B and C_{in} to compute the two 1-bit outputs i.e. sum and C_{out} which are given by,

$$\begin{aligned} \text{Sum} &= A \text{ XOR } B \text{ XOR } C_{in} \\ C_{out} &= A \cdot B + C_{in}(A \text{ XOR } B) \end{aligned}$$

Basically we proposed 8 transistor full adder with an extra transistor M9 to improve the performance of 8 transistor full adder cell. The C_{out} is implemented using 2 transistor multiplexer and the Sum is obtained from a cascaded XORing of three inputs with an extra transistor i.e. M9. Here, the truth table is divided into two parts, one for $A=0$ and other for $A=1$ rather than conventional sum module. For $A=0$, sum can be implemented by XORing input B and C_{in} and for $A=1$, it can be given by XNORing inputs B and C_{in} . Here, we proposed the use of self biasing or it can be also explained as body biasing. In this technique, the body of transistors giving output as sum and carryout are biased with the input. This self biasing helps in optimizing the circuit power consumption. The power consumption of self biased circuit is reduced as compared to the unbiased one.

IV. SIMULATION RESULTS

Tanner EDA 13.00 is used for the evaluation of proposed system. Each block of design is simulated in S-edit and waveforms are analysed using W-edit. The entire simulation is done in 180nm CMOS technology with supply voltage of 5V. The results are compared with different full adder designs. The compared output, truth table and simulation results are given here.

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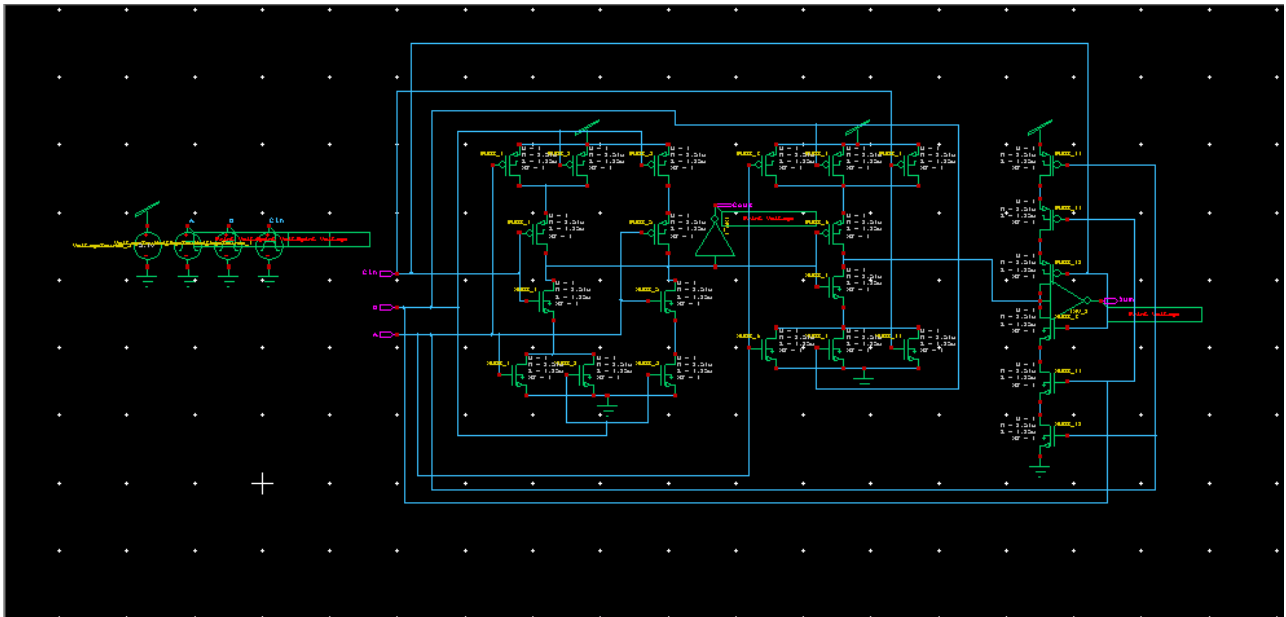


Fig. 9: Schematic of Conventional Mirror Adder

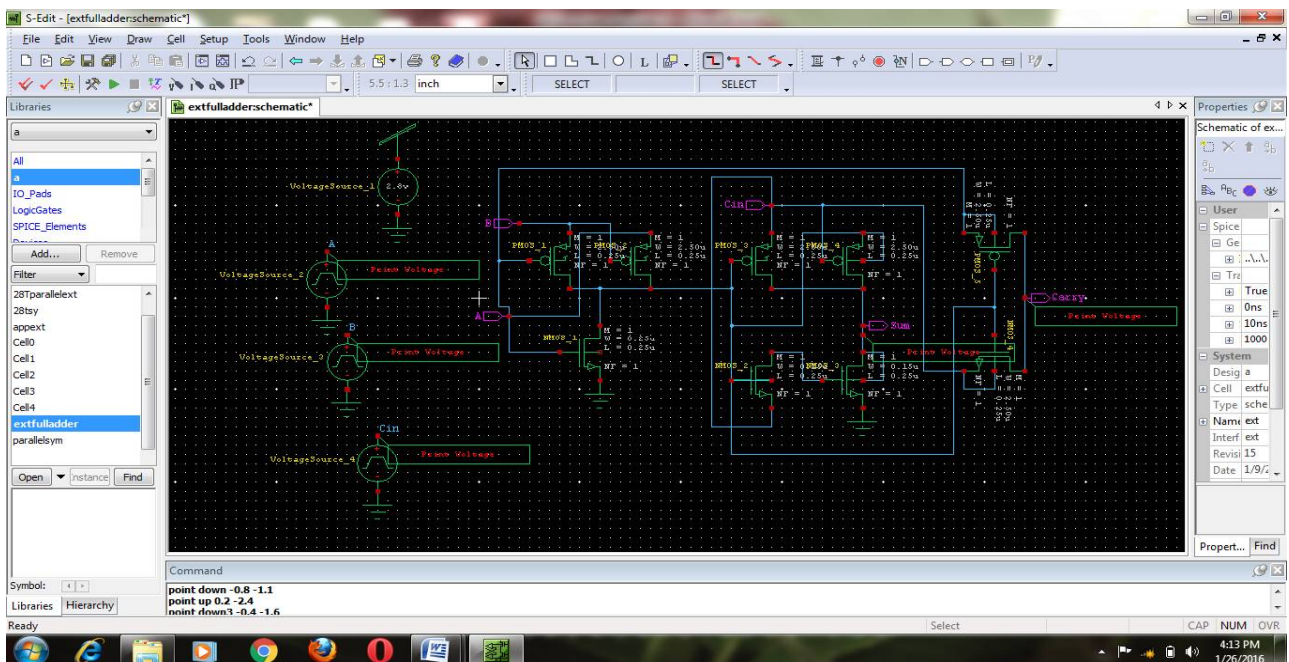


Fig.10: 9 transistor Full Adder with Self Biasing

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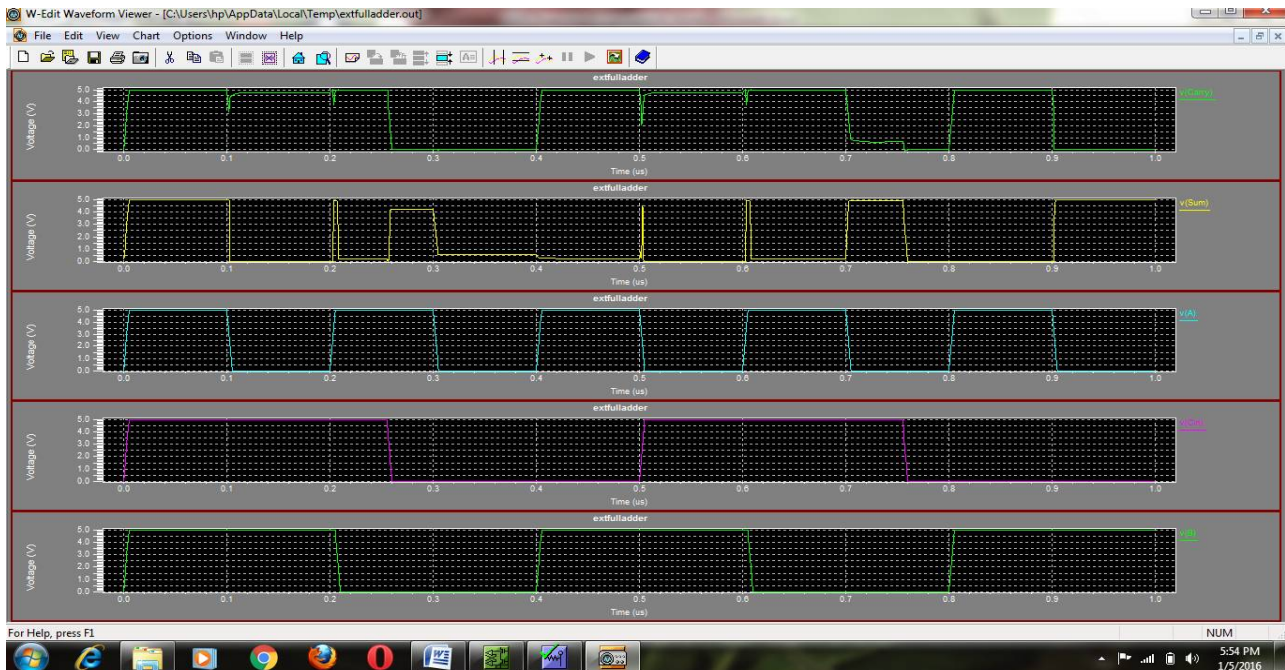


Fig.11: 9 Transistor Full Adder with Self Biasing Simulation Result

The above given figures shows the schematic of conventional mirror adder and proposed 9 transistor full adder and its output waveform in fig. Number 9, 10 and 11. Fig. 12 shows the voltage vs power dissipation graph for different full adder designs. The given tables 1 and 2 shares the truth table for one bit full adder and power dissipation and also the transistor count for various CMOS full adder cells respectively.

Table 1: Truth table For Full Adder

A	B	C _{IN}	Sum	Carryout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table2:Parameters of Different Full Adder

Circuits	Power Consumption (W)	Transistor Count
Conventional Mirror Adder	5.427069e-005	24
Approximation 1	1.162739e-006	16
Approximation 2	2.448304e-005	14
Approximation 3	3.176605e-007	11
Approximation 4	1.751802e-006	11
9 Transistor Full Adder	3.085600e-008	9

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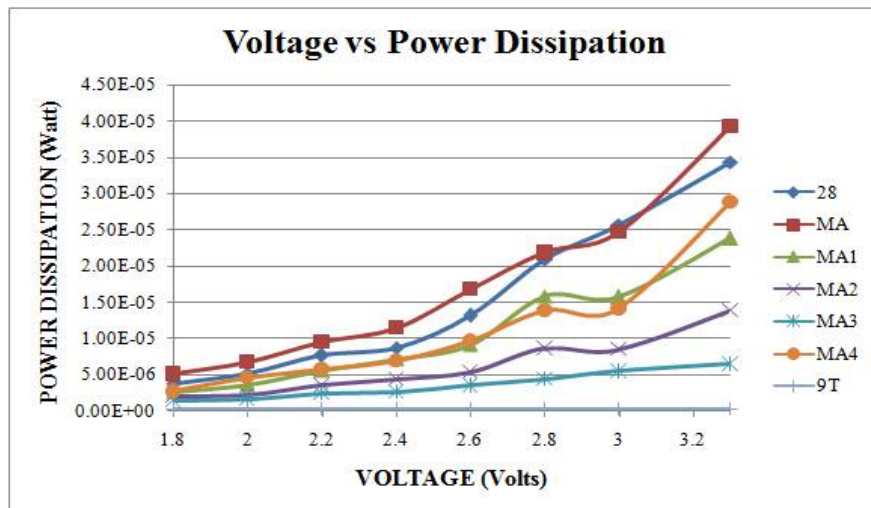


Fig.12: Power Dissipation of different full adder circuits with different operating voltages

V. CONCLUSION

In this paper, we proposed some inaccurate i.e. approximate full adders that can be utilized in various low power applications. Our approach differed from previous work and the reduced number of transistors helped in reducing the switching capacitance. For performance validation, Tanner simulations were conducted on FAs implemented with TSMC 018 CMOS process technology in aspects of power consumption, delay time. The proposed circuit gives highest power optimization among all previous full adder and it also helped in faster operation. The enhancement can be done with 6 transistor full adder in future followed by this work.

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International Journal of Innovative Research in Science, Engineering and Technology

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BIOGRAPHY



Astha Sharma received the B.E. degree in Electronics & Telecommunication from CSVTU, Chhattisgarh, India in 2014 and currently pursuing M.Tech in VLSI & Embedded System from DIMAT, Raipur Chhattisgarh, India. Her current research include a new configurable full adder for low power applications.



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